

Preliminary **1.9GHz 20 W Flange Ceramic Packaged GaAs Power FETs**
FEATURES

- 20 W Typical Power at 1.9 GHz
- 11 dB Typical Linear Power Gain at 1.9 GHz
- High Linearity:
IP3 = 52 dBm Typical
- High Power Added Efficiency:
Nominal PAE of 40 %
- Suitable for High Reliability Application
- $L_g = 1 \mu\text{m}$, $W_g = 50 \text{ mm}$
- 100 % DC and RF Tested
- Flange Ceramic Package

PHOTO ENLARGEMENT

DESCRIPTION

The TC2997B is a packaged Pseudomorphic High Electron Mobility Transistor (PHEMT) power transistor. The flange ceramic package provides the best thermal conductivity for the GaAs FET. All devices are 100% DC and RF tested to assure consistent quality. Typical applications include high dynamic range power amplifier for commercial applications.

ELECTRICAL SPECIFICATIONS (@ 1.9 GHz)

Symbol	CONDITIONS	MIN	TYP	MAX	UNIT
P_{1dB}	Output Power at 1dB Gain Compression Point $V_{DS} = 10.5 \text{ V}$, $I_{DS} = 5 \text{ A}$	42	43		dBm
G_L	Linear Power Gain $V_{DS} = 10.5 \text{ V}$, $I_{DS} = 5 \text{ A}$	11	12		dB
IP3	Intercept Point of the 3 rd -order Intermodulation $V_{DS} = 10.5 \text{ V}$, $I_{DS} = 5 \text{ A}$, * $P_{SCL} = 32 \text{ dBm}$		52		dBm
PAE	Power Added Efficiency at 1dB Compression Power		40		%
I_{DSS}	Saturated Drain-Source Current at $V_{DS} = 2 \text{ V}$, $V_{GS} = 0 \text{ V}$		12.5		A
g_m	Transconductance at $V_{DS} = 2 \text{ V}$, $V_{GS} = 0 \text{ V}$		9000		mS
V_P	Pinch-off Voltage at $V_{DS} = 2 \text{ V}$, $I_D = 60 \text{ mA}$		-1.7		Volts
BV_{DGO}	Drain-Gate Breakdown Voltage at $I_{DGO} = 15 \text{ mA}$	20	22		Volts
R_{th}	Thermal Resistance		0.9		°C/W

* P_{SCL} : Output Power of Single Carrier Level.

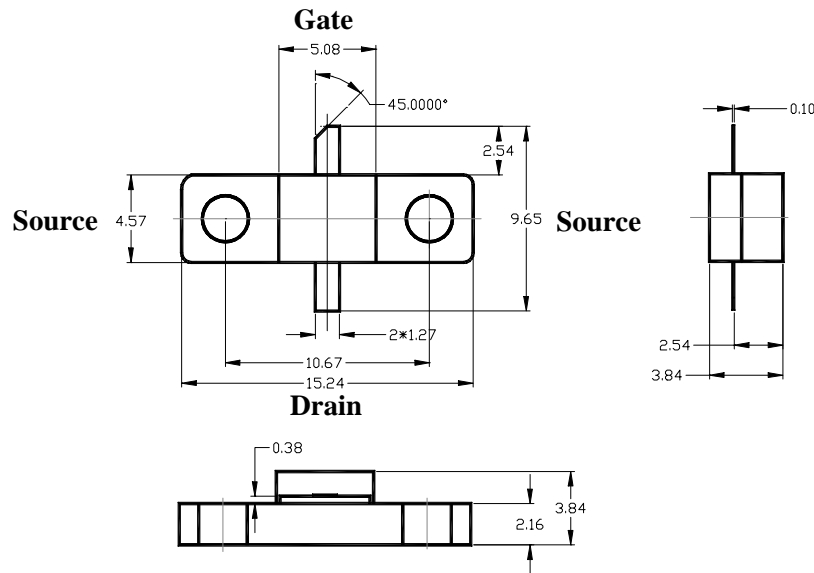
ABSOLUTE MAXIMUM RATINGS at 25 °C

Symbol	Parameter	Rating
V _{DS}	Drain-Source Voltage	12 V
V _{GS}	Gate-Source Voltage	-5 V
I _{DS}	Drain Current	I _{DSS}
P _{in}	RF Input Power, CW	37 dBm
P _T	Continuous Dissipation	100 W
T _{CH}	Channel Temperature	175 °C
T _{STG}	Storage Temperature	- 65 °C to +175 °C

HANDLING PRECAUTIONS:

The user must operate in a clean, dry environment. Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. The static discharge must be less than 300V.

FLANGE PACKAGE OUTLINE (in mm)



TYPICAL COMMON SOURCE SCATTERING PARAMETERS (V_D = 10.5 V, I_D = 5 A)

FREQUENCY (GHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
1	0.98447	175.60	0.89405	58.716	0.004436	-11.953	0.83047	-171.23
2	0.89499	175.92	1.01350	-35.168	0.011258	-80.437	0.96855	-173.25
3	0.99590	170.70	0.12798	-99.501	0.002725	-127.56	0.98934	176.29
4	0.99889	165.88	0.04273	-109.58	0.001526	-127.53	0.98926	171.49
5	0.99929	161.45	0.02065	-115.98	0.001113	-127.40	0.99039	167.26
6	0.99934	157.00	0.01208	-121.61	0.000908	-128.39	0.99112	163.24

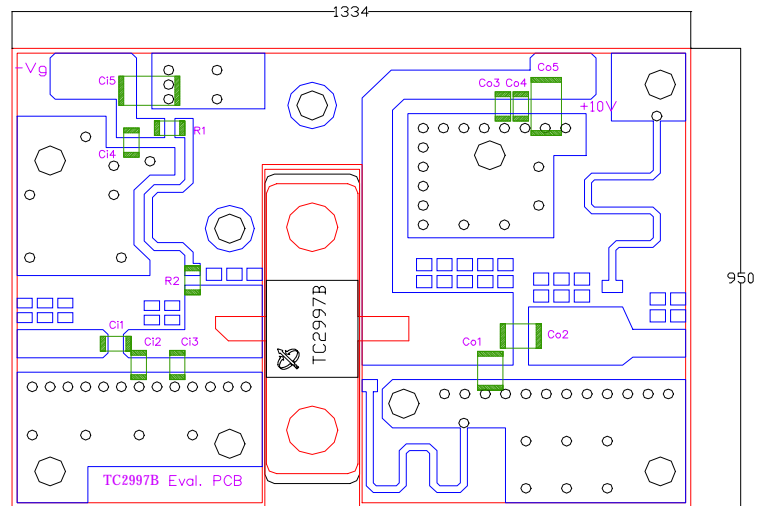
EVALUATION BOARD

PCB Material: FR4

ER = 4.6

Thickness = 31 mil

Unit: mil



Part Type	Reference Designator	Description	Manufacturer
Resistor	R1	10 ohm 0603	
Resistor	R2	0 ohm 0603	
Capacitor	Ci1	1.2 pF 0603	Murata
Capacitor	Ci2	1.0 pF 0603	Murata
Capacitor	Ci3	1.5 pF 0603	Murata
Capacitor	Ci4	1000 pF 0603	Murata
Capacitor	Ci5	10 uF 1206	Murata
Capacitor	Co1	2.2 pF 1212	Temex
Capacitor	Co2	1.5 pF 1212	Temex
Capacitor	Co3	1000 pF 0603	Murata
Capacitor	Co4	0.1 uF 0603	Murata
Capacitor	Co5	10 uF 1206	Murata